

# Shahriar Rizvi

B.Sc. Candidate in CSE | IEEE-Published Researcher | Teaching & Research in Computing Systems

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[Portfolio](#) | [LinkedIn](#) | [GitHub](#) | [ResearchGate](#) | [Google Scholar](#) | [ORCID](#)

Final-semester B.Sc. CSE candidate at Rajshahi University of Engineering & Technology, with academic requirements expected to be completed by July 2026. IEEE-published researcher with hands-on work in FPGA acceleration, RTL/VLSI, quantum computing, AI, computer architecture, operating systems, computer graphics, and positioning systems. Prepared to contribute to undergraduate teaching, laboratory instruction, student mentoring, and research development while explaining technical topics through clear “what, why, and how” connections to modern technology.

## Education

<b>B.Sc. in CSE</b>	Rajshahi University of Engineering & Technology (RUET), Bangladesh (Final semester; academic requirements expected to be completed by July 2026.)	2026	CGPA: 3.88/4.00
<b>HSC, Science</b>	Government Edward College, Pabna, Bangladesh	2020	GPA: 5.00/5.00
<b>SSC, Science</b>	Pabna Zilla School, Pabna, Bangladesh	2018	GPA: 5.00/5.00

## Research Publications

**FPGA Acceleration of Quantum Circuit Primitives: Fixed-Point Microcoded Design and CPU Comparison**  
Shahriar Rizvi and Md. Nazrul Islam Mondal. *IEEE ICECTE 2026*. DOI: [10.1109/ICECTE69292.2026.11429464](https://doi.org/10.1109/ICECTE69292.2026.11429464)

**Beyond Artifacts: Semantic Deepfake Detection and Digital Provenance Tracking with Multimodal Large Language Models**  
Jabunnesa Jahan Sara, Shahriar Rizvi, and Tasfia Jannat Tasfi. *IEEE ICCIT 2025*. DOI: [10.1109/ICIT68739.2025.11490141](https://doi.org/10.1109/ICIT68739.2025.11490141)

## Ongoing Thesis and Research Direction

**FPGA-Based Quantum Neural Network Accelerator: A Quantum-Inspired VLSI Design Approach** Thesis / Ongoing

- Supervisor: Prof. Dr. Md. Nazrul Islam Mondal, Department of CSE, RUET.
- Working on quantum-inspired acceleration using RTL design, FPGA prototyping, fixed-point datapaths, microcoded control, simulation-based validation, and open-source EDA/VLSI-style evaluation.

**DSP-Assisted Hybrid Wi-Fi and Visible Light Positioning for Indoor Localization** Conference Research / Ongoing

- Exploring low-cost indoor positioning by combining Wi-Fi signal behavior, visible light positioning, DSP-based feature processing, and reproducible experimental analysis for communication/signal-processing research.

## Selected Technical Projects

**SigmaCore RISC-V CPU Design** [GitHub](#)

- Building a 32-bit multicycle RISC-V CPU in SystemVerilog with modular ALU, control unit, register file, memory, instruction decoder, sign extender, and top-level testbench.
- Uses FSM-based control and a smart-monitor testbench with console traces and waveform debugging through Icarus Verilog and GTKWave.

**SigmaCore Operating System (Ongoing)** [GitHub](#)

- Developing a small operating system from scratch with low-level Assembly-focused boot components, connecting OS concepts with processor architecture and bare-metal system design.

**Bezier Breakout: Curve Ball Arena** [GitHub](#)

- Built a C++17 OpenGL/GLUT computer-graphics game using primitives and procedural visuals, with paddle control, levels, camera/help controls, sound fallback, and no external game engine.

**AI-Powered Attendance System** [GitHub](#)

- Built a Python-based facial-recognition attendance system with GUI, model training, real-time camera recognition, CSV attendance import/export, and student attendance reporting.

**BoiKothon – Book Review Sharing Platform** [GitHub](#)

- Developed a Django-based book-community web application with authentication, group creation/joining, post discussions, responsive design, and SQLite-backed development workflow.

## Technical Skills

<b>Programming</b>	C, C++, Python, SQL, JavaScript/Node.js, LaTeX
<b>Hardware / RTL</b>	Verilog, SystemVerilog, RTL design, finite-state machines, CPU datapath, FPGA-oriented design
<b>Systems / Graphics</b>	Bare-metal programming, Assembly fundamentals, operating-system concepts, OpenGL/GLUT, computer graphics
<b>AI / ML</b>	Classification, feature engineering, model evaluation, explainable AI basics, computer vision basics
<b>Signal / Positioning</b>	DSP fundamentals, signal-feature analysis, Wi-Fi sensing, visible light positioning, indoor localization
<b>Tools</b>	Git, GitHub, Linux/Ubuntu, Icarus Verilog, Verilator, GTKWave, Vivado, Jupyter/Colab
<b>Web / Database</b>	Django, Laravel, backend fundamentals, SQL database design, SQLite/MySQL
<b>Networking</b>	IP addressing, subnetting, VLAN concepts, RIP/OSPF basics, Cisco Packet Tracer

## Honors and Achievements

- **Champion**, VLSITHON 2024, RTL Section, ULKASEMI.
- **Quantum Excellence**, IBM Qiskit Global Summer School 2025.
- **Government Technical Scholarship** recipient for all 4 years of undergraduate study.
- **Bronze Honour**, International Youth Math Challenge, 2024.
- **1st Prize and Funding Recipient**, University Innovation Hub Program (UIHP), 2025.
- **Champion**, HULT Prize on Campus RUET, 2023.
- **Champion**, National High School Programming Contest, 2016.
- **Champion**, Science Olympiad, 2018 and 2019.
- **Champion**, Creative Talent Hunt Regional, 2019.
- Earlier academic distinctions: **Bangladesh Math Olympiad** Regional Runners Up awards in 2017 and 2019; 1st Runner-up, Science Fair 2020.

## Teaching Experience and Teaching Readiness

### Competitive Programming Instructor / Mentor

1+ Years

RUET Analytical and Programming Lab (RAPL)

- Mentored 100+ junior students through RAPL activities and peer-learning sessions in C/C++, algorithms, debugging, and contest-oriented problem solving.

### Private Tutor / Academic Mentor

5+ Years

SSC, HSC, Engineering Admission Test, and University-Level Students

- Delivered long-term academic mentoring across SSC, HSC, engineering admission preparation, and selected university-level topics, emphasizing conceptual understanding, step-by-step problem solving, and examination strategy.

### Teaching Readiness

Courses, Laboratories, Teaching Approach, and Medium of Instruction

- Prepared to teach core undergraduate CSE courses: Structured Programming, OOP, Data Structures, Algorithms, Digital Logic Design, Computer Architecture, Database Systems, Operating Systems, Computer Networks, AI, and Software Engineering.
- Ready to support programming, Verilog/SystemVerilog, digital logic, computer architecture, database, AI/ML, graphics, and Linux/Git-based project labs.
- Concept-first teaching approach using examples, intuition, hands-on practice, and modern technology use cases; comfortable instructing technical courses and labs in English.

## Management Experience and Extracurricular Activities

### Class Representative and Coordinator

2023 – 2025

Department of CSE, RUET

- Served as a regular communication bridge between faculty members and students for academic scheduling, course updates, notices, and departmental coordination.

### Vice President

2025 – Present

RUET Computing Society

- Supported computing culture, peer learning, student engagement, and technical-event coordination within RUET.

### Campus Ambassador

2025 – 2026

ULKASEMI Private LTD

- Promoted semiconductor, RTL, and VLSI career awareness among students through campus-level engagement.

### Official Ambassador

2025

International Computer Science Competition (ICSC)

- Encouraged student participation in international computer science, algorithmic, and problem-solving competitions.

### Joint Secretary

2025 – Present

Pabna District Association, RUET

- Assisted in community coordination, student networking, event organization, and association-level communication.

## Research and Academic Interests

Computer Architecture; FPGA Acceleration; RTL and VLSI Design; Operating Systems; Computer Graphics; Quantum Computing; Quantum-Inspired Machine Learning; DSP; Wi-Fi Sensing; Visible Light Positioning; Artificial Intelligence; Explainable AI; Computer Networks; Embedded Systems.

## References

### Prof. Dr. Md. Nazrul Islam Mondal

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